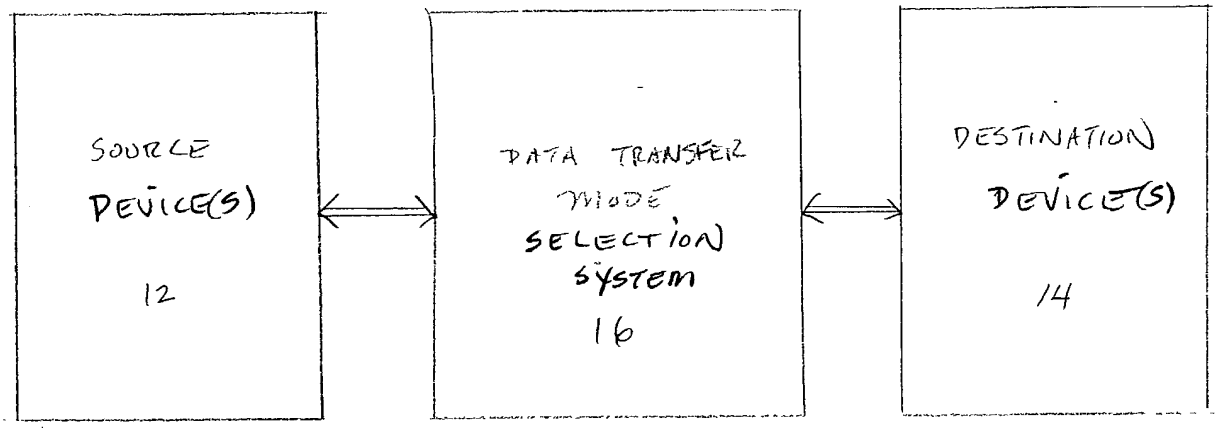
SOURCE
DEVICE(S)
12
DATA TRANSFER
MODE
SELECTION
SYSTEM
16
DESTINATION
DEVICE(S)
14

105

FIG. 1

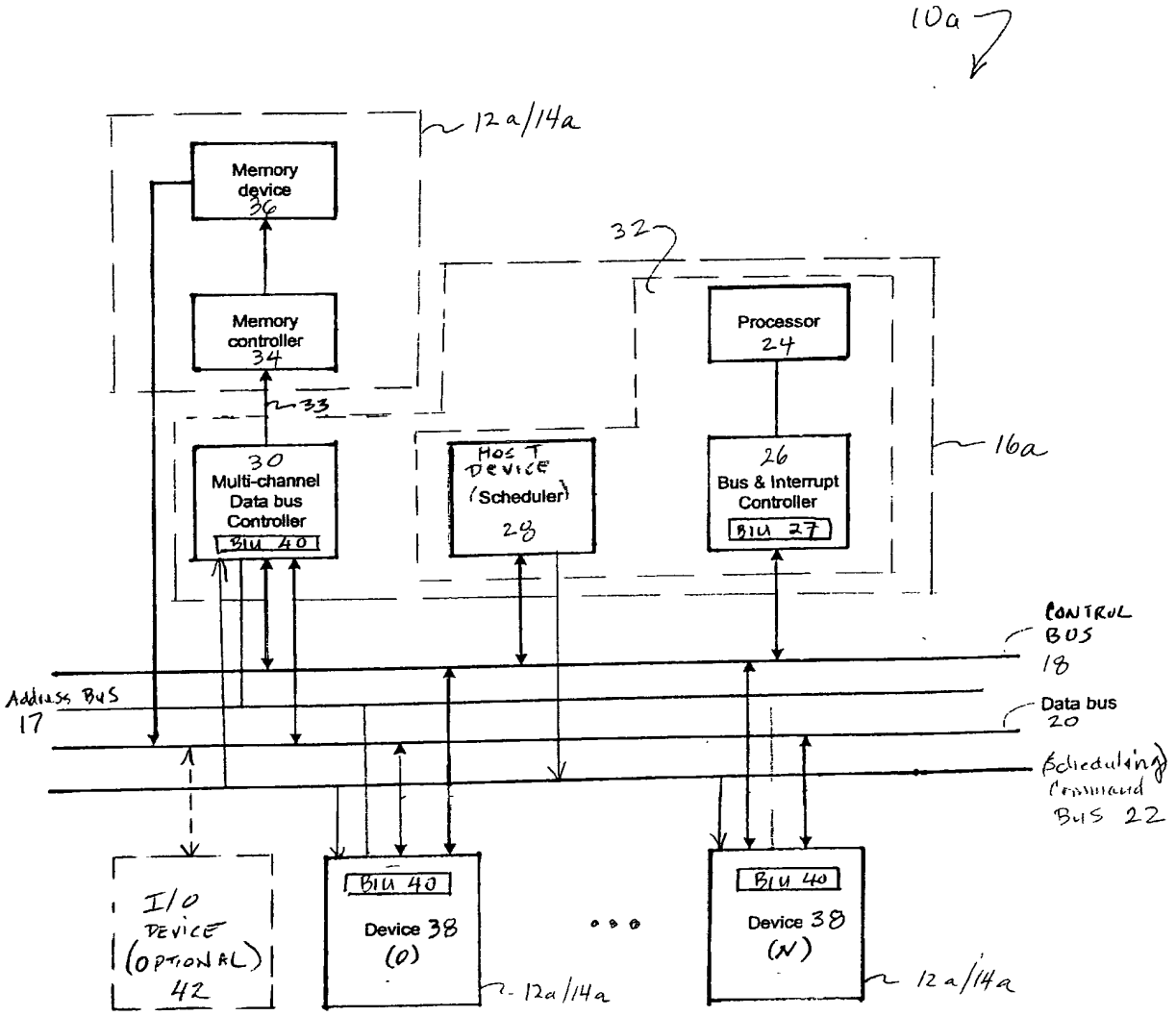
10a
12a/14a
Memory device 36
Memory controller 34
33
32
Processor 24
30 Multi-channel Data bus Controller
BIU 40
Host Device (Scheduler) 28
26 Bus & Interrupt Controller
BIU 27
16a
CONTROL BUS 18
Address Bus 17
Data bus 20
Scheduling Command Bus 22
I/O DEVICE (OPTIONAL) 42
BIU 40
Device 38 (0)
12a/14a
BIU 40
Device 38 (N)
12a/14a

FIG. 2

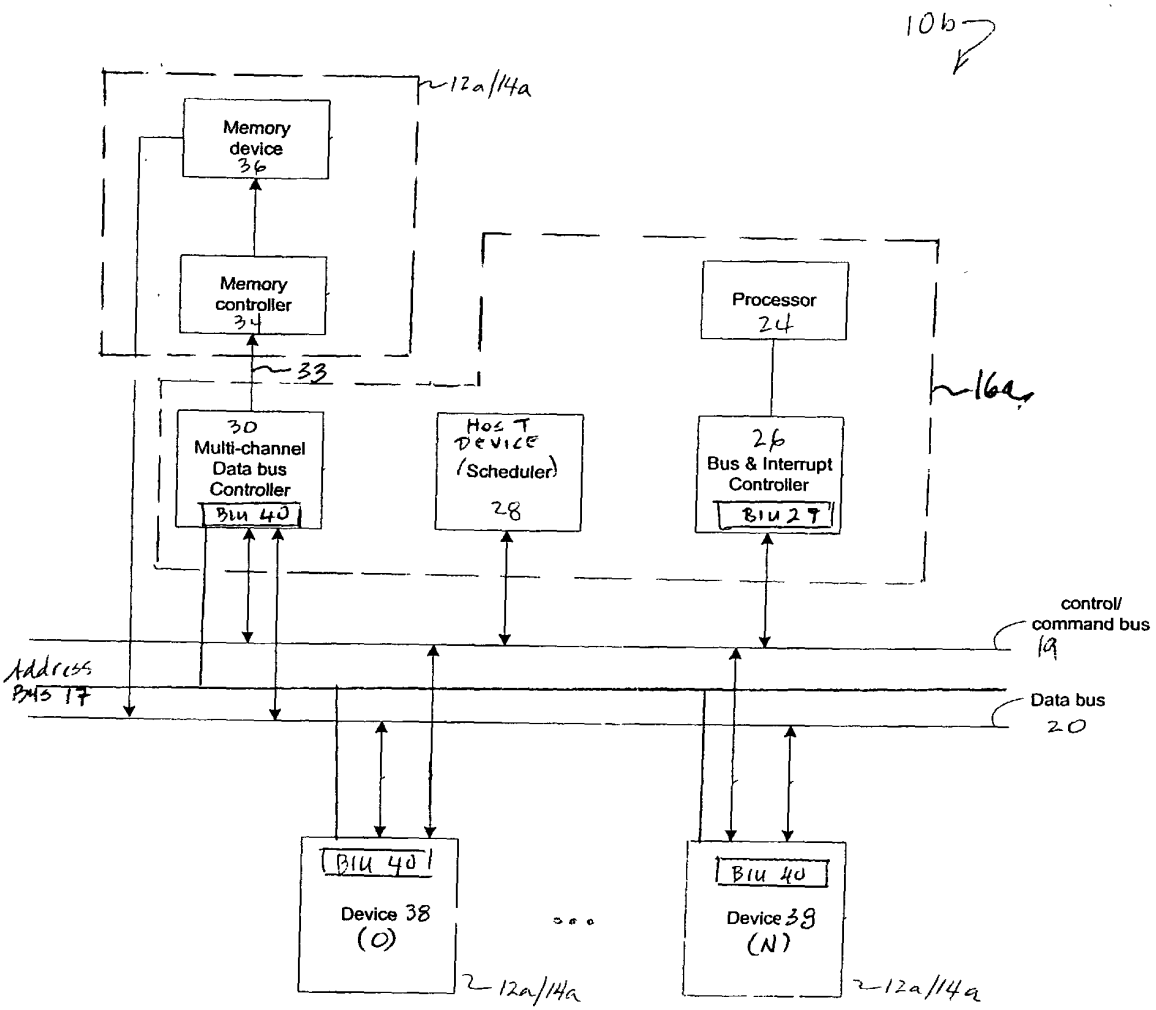
10b
12a/14a
Memory device 36
Memory controller 34
33
16a
Processor 24
30 Multi-channel Data bus Controller
BIU 40
Host Device (Scheduler) 28
26 Bus & Interrupt Controller
BIU 27
control/ command bus 19
Address Bus 17
Data bus 20
BIU 40
Device 38 (0)
12a/14a
BIU 40
Device 39 (N)
12a/14a

FIG. 3

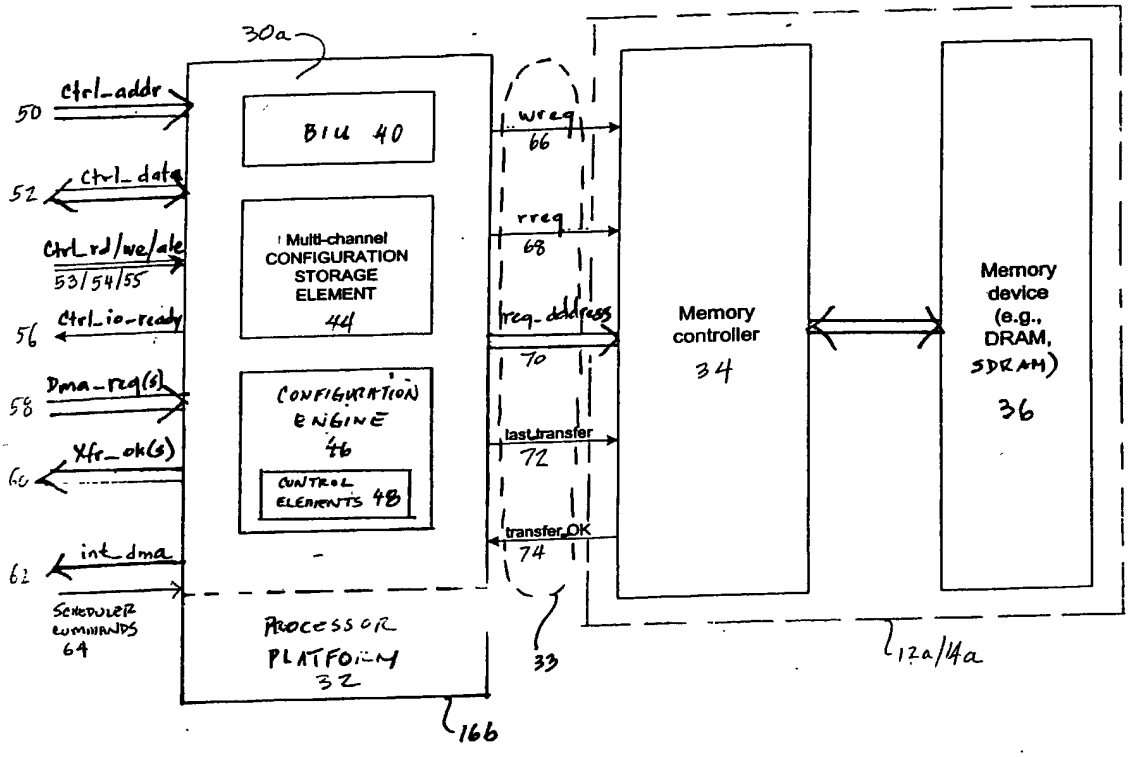
30a
Ctrl_addr
50
Ctrl_data
52
Ctrl_rd/we/ale
53/54/55
Ctrl_io_ready
56
Dma_req(s)
58
Xfr_ok(s)
60
int_dma
62
SCHEDULER COMMANDS 64
BIU 40
Multi-channel CONFIGURATION STORAGE ELEMENT 44
CONFIGURATION ENGINE 46
CONTROL ELEMENTS 48
PROCESSOR PLATFORM 32
166
wreq 66
rreq 68
req_address 70
last_transfer 72
transfer_OK 74
33
Memory controller 34
Memory device (e.g., DRAM, SDRAM) 36
12a/14a

FIG. 4

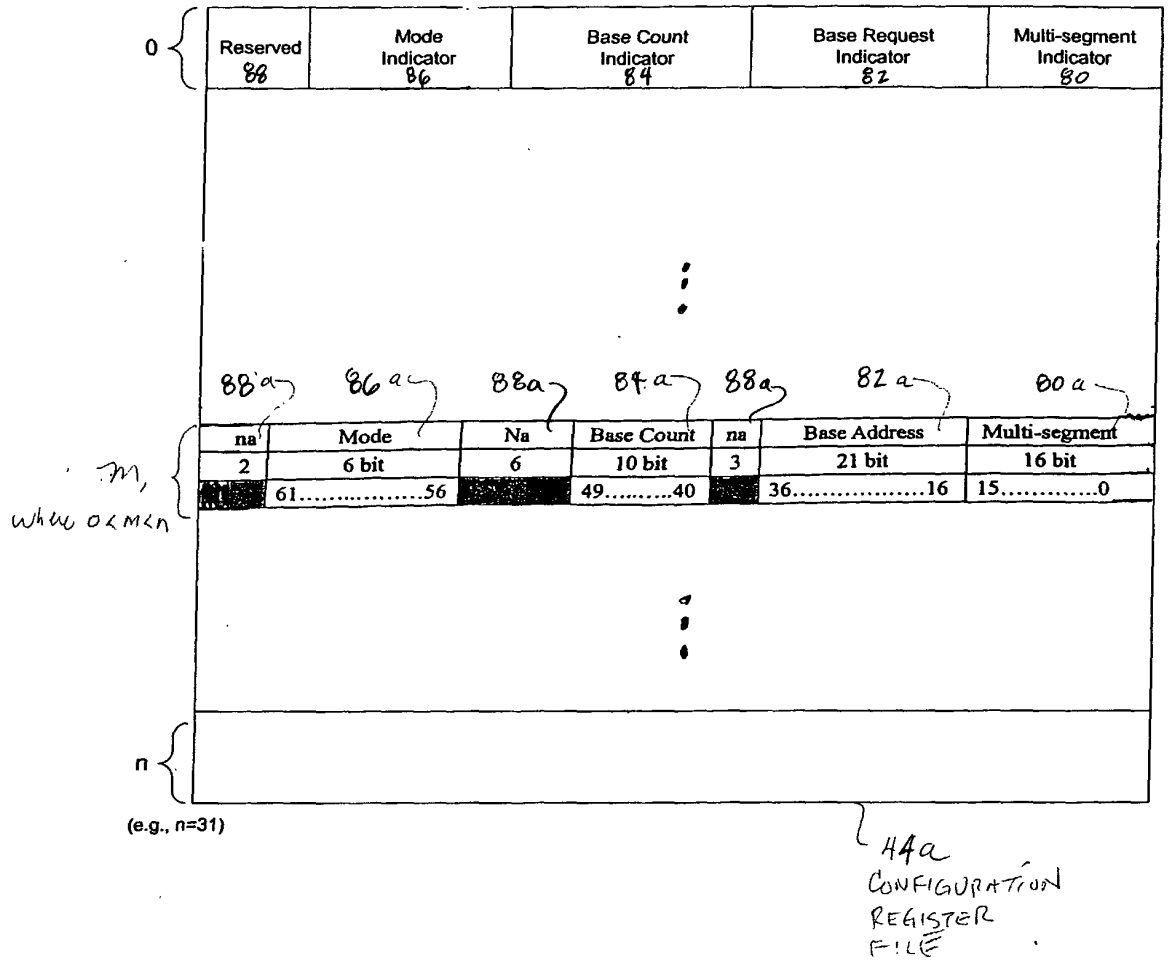
0
Reserved 88
Mode Indicator 86
Base Count Indicator 84
Base Request Indicator 82
Multi-segment Indicator 80
88a
86a
88a
84a
88a
82a
80a
na
Mode
Na
Base Count
na
Base Address
Multi-segment
2
6 bit
6
10 bit
3
21 bit
16 bit
61.....56
49.....40
36.....16
15.....0
m, where 0<m<n
n
(e.g., n=31)
44a
CONFIGURATION REGISTER FILE

FIG. 5

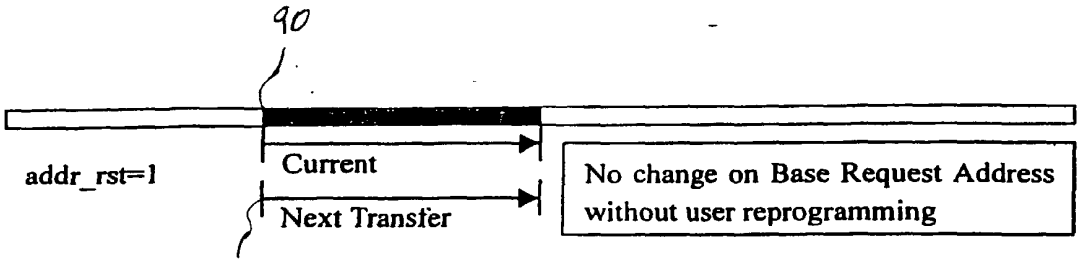

Fig. 6A

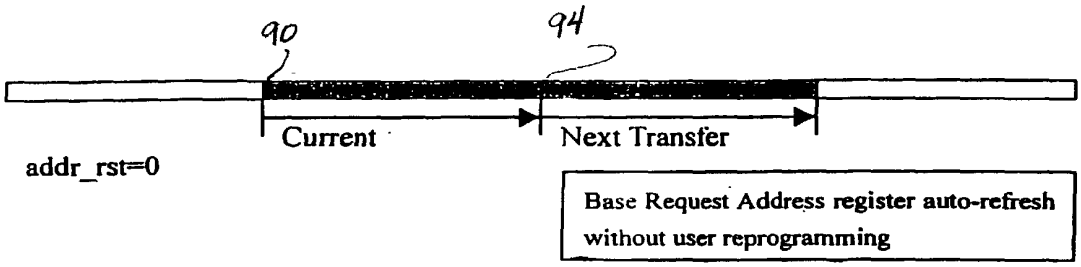

Fig. 6B

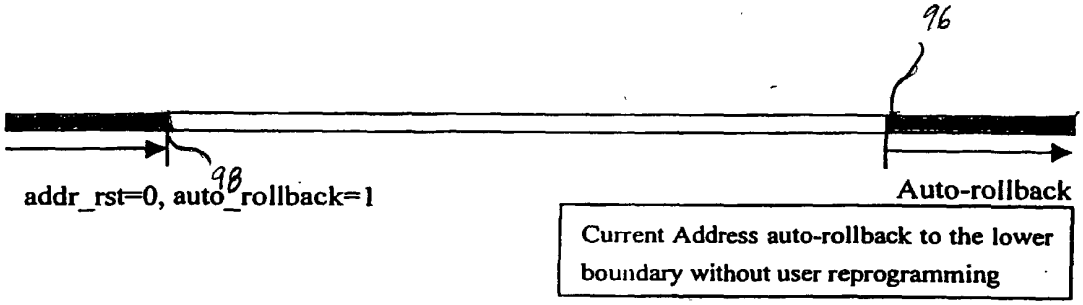

Fig. 6C

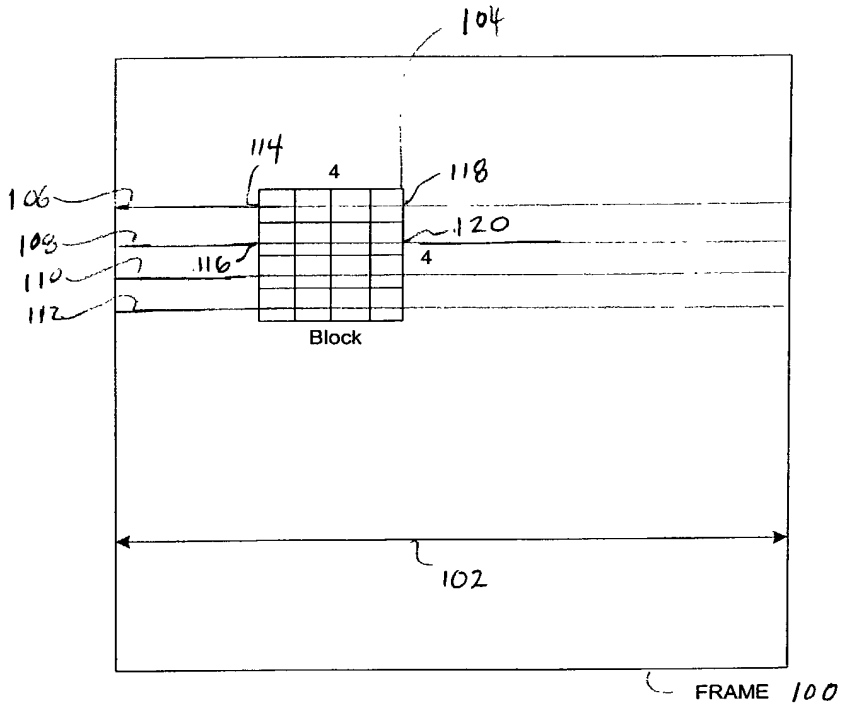

FIG. 7

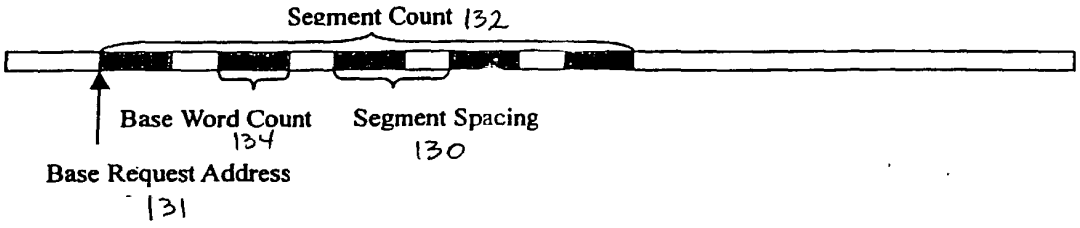
Segment Count 132
Base Word Count
134
Segment Spacing
130
Base Request Address
131

Fig. 8

SIGNAL FLOW DIAGRAM
FOR VIRTUAL CHANNEL MODE

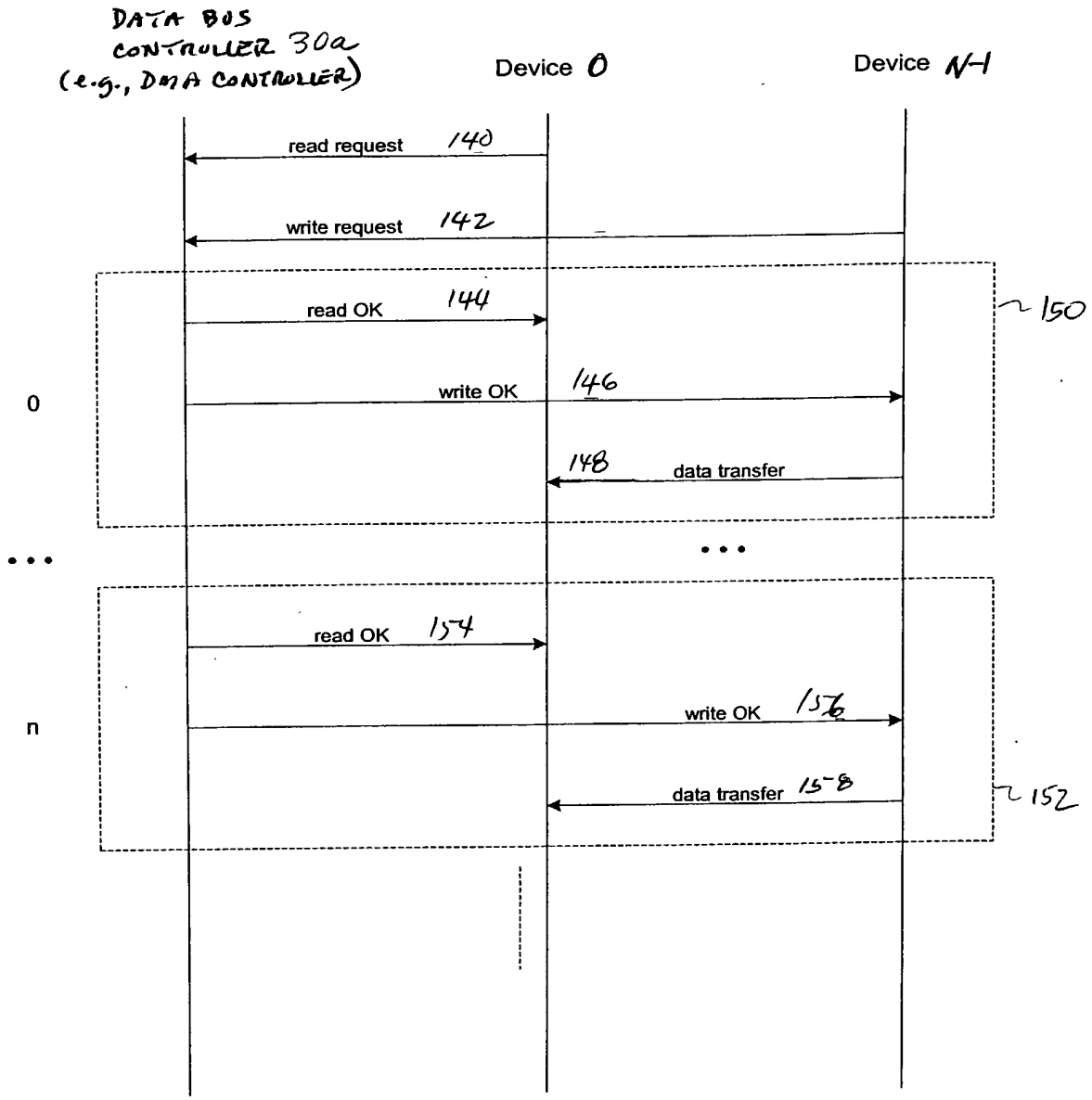

FIG. 9

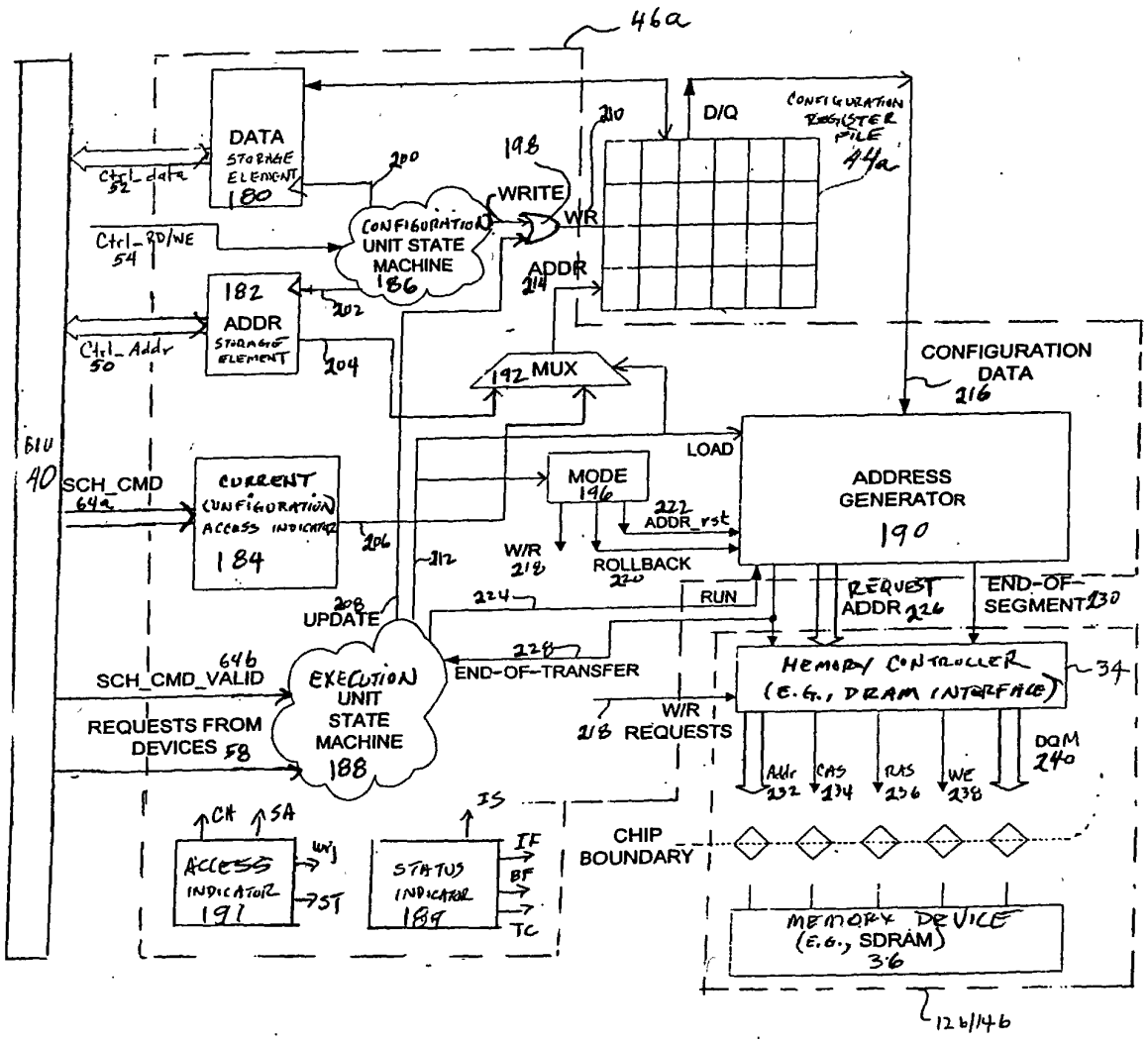
46a
DATA STORAGE ELEMENT 180
Ctrl_data 52
200
198
WRITE
WR
CONFIGURATION UNIT STATE MACHINE 186
Ctrl_RD/WE 54
ADDR 214
210
D/Q
CONFIGURATION REGISTER FILE 44a
182 ADDR STORAGE ELEMENT
202
Ctrl_Addr 50
204
192 MUX
CONFIGURATION DATA 216
BIU 40
SCH_CMD 64a
CURRENT CONFIGURATION ACCESS INDICATOR 184
206
212
MODE 196
LOAD
ADDRESS GENERATOR 190
222 ADDR_rst
W/R 218
ROLLBACK 220
224
RUN
REQUEST ADDR 226
END-OF-SEGMENT 230
208 UPDATE
228 END-OF-TRANSFER
64b SCH_CMD_VALID
EXECUTION UNIT STATE MACHINE 188
REQUESTS FROM DEVICES 58
W/R 218 REQUESTS
MEMORY CONTROLLER (E.G., DRAM INTERFACE) 34
Addr 232
CAS 234
RAS 236
WE 238
DQM 240
CH
SA
IS
ACCESS INDICATOR 191
WI
TST
STATUS INDICATOR 189
IF
BF
TC
CHIP BOUNDARY
MEMORY DEVICE (E.G., SDRAM) 36
126/146
30a

FIG. 10

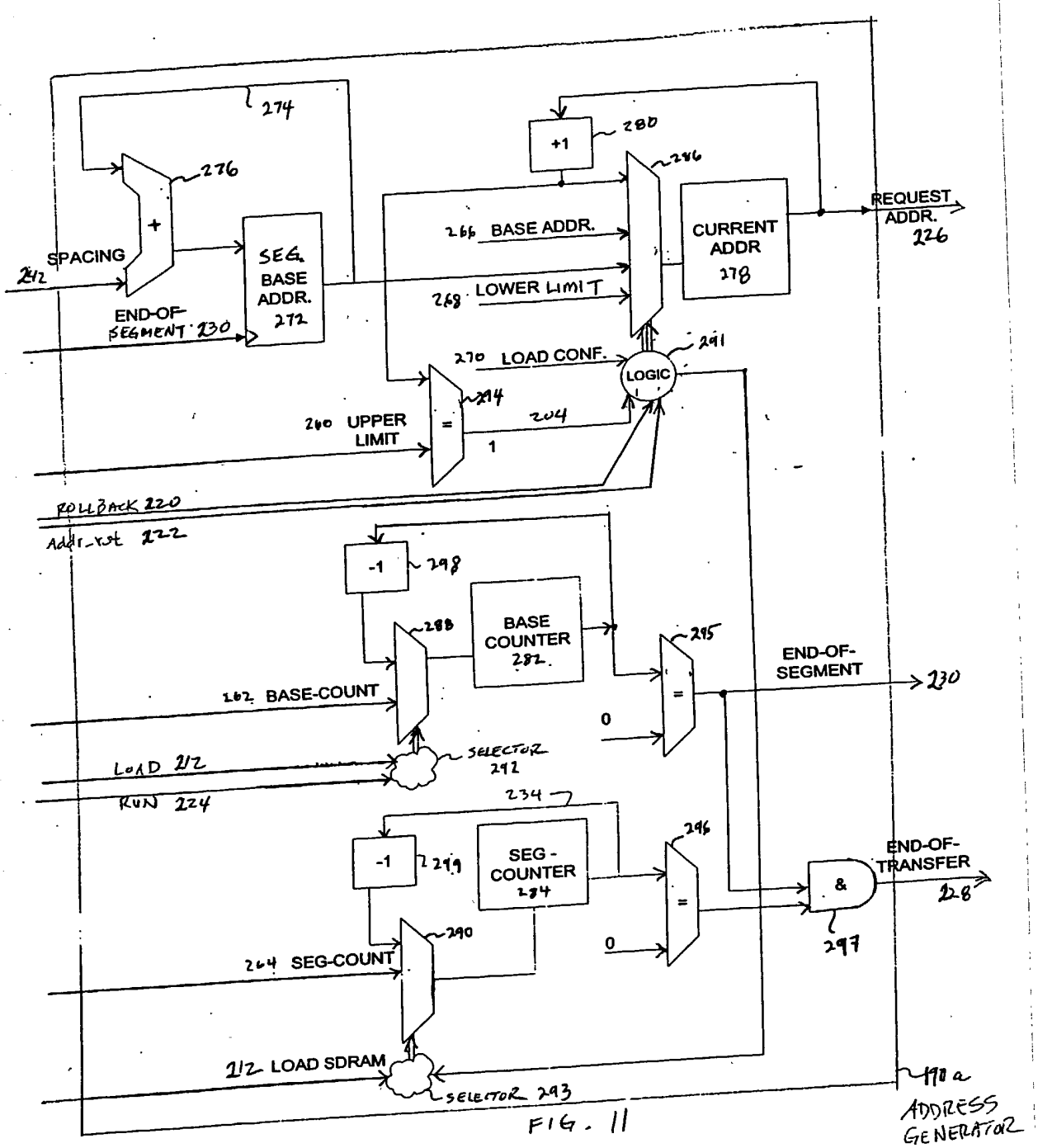
274
276
+
SPACING
242
END-OF-SEGMENT 230
SEG. BASE ADDR. 272
+1
280
286
266 BASE ADDR.
268 LOWER LIMIT
CURRENT ADDR 278
REQUEST ADDR. 226
270 LOAD CONF.
LOGIC
291
260 UPPER LIMIT
=
294
204
1
ROLLBACK 220
Addr_out 222
-1
298
288
BASE COUNTER 282
295
END-OF-SEGMENT
230
262 BASE-COUNT
0
LOAD 212
RUN 224
SELECTOR 292
234
-1
299
SEG-COUNTER 284
296
END-OF-TRANSFER
228
&
297
264 SEG-COUNT
290
212 LOAD SDRAM
SELECTOR 293
190a
ADDRESS GENERATOR

FIG. 11

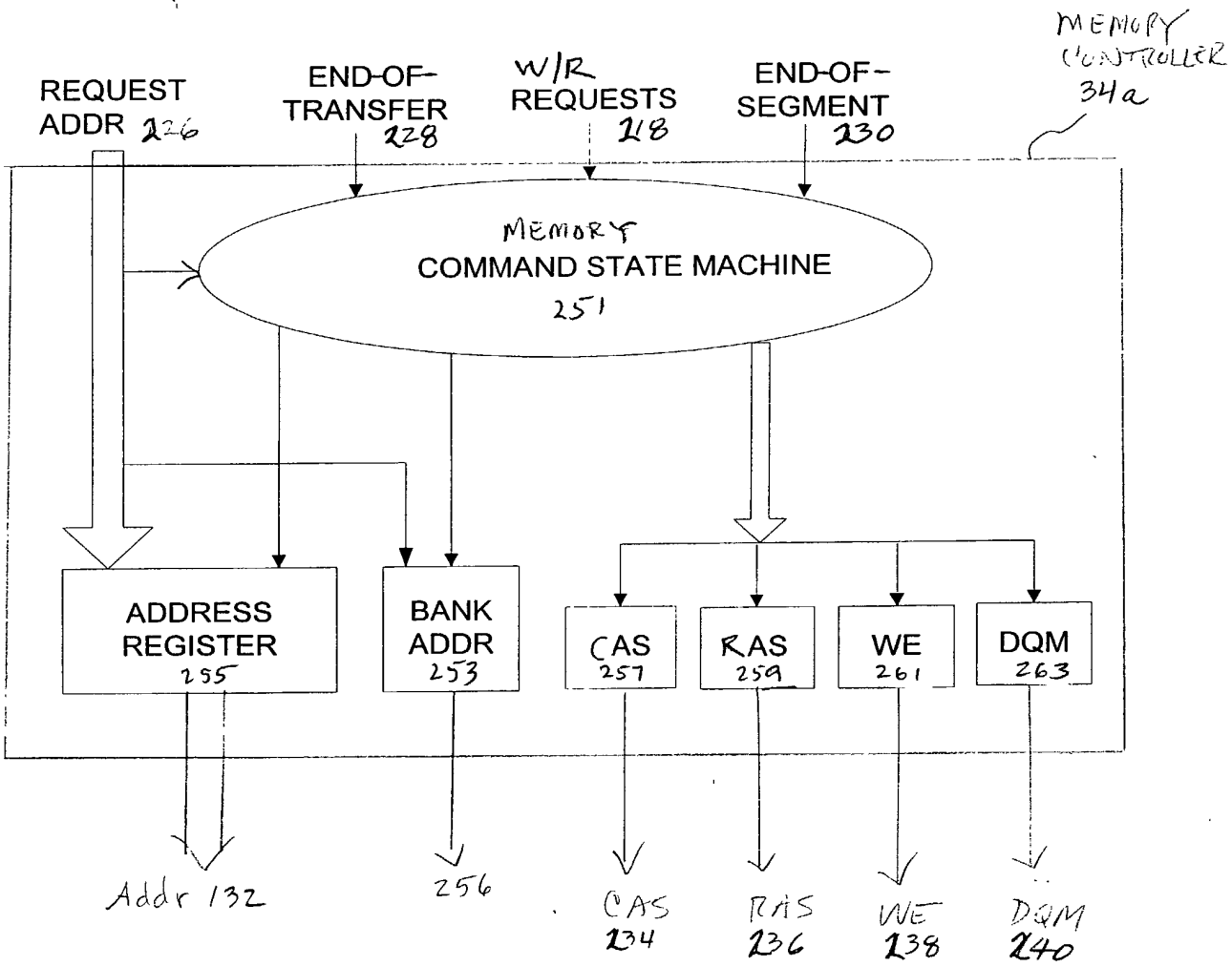
REQUEST ADDR 226
END-OF-TRANSFER 228
W/R REQUESTS 218
END-OF-SEGMENT 230
MEMORY CONTROLLER 34a
MEMORY COMMAND STATE MACHINE 251
ADDRESS REGISTER 255
BANK ADDR 253
CAS 257
RAS 259
WE 261
DQM 263
Addr 132
256
CAS 234
RAS 236
WE 238
DQM 240

FIG. 12

300

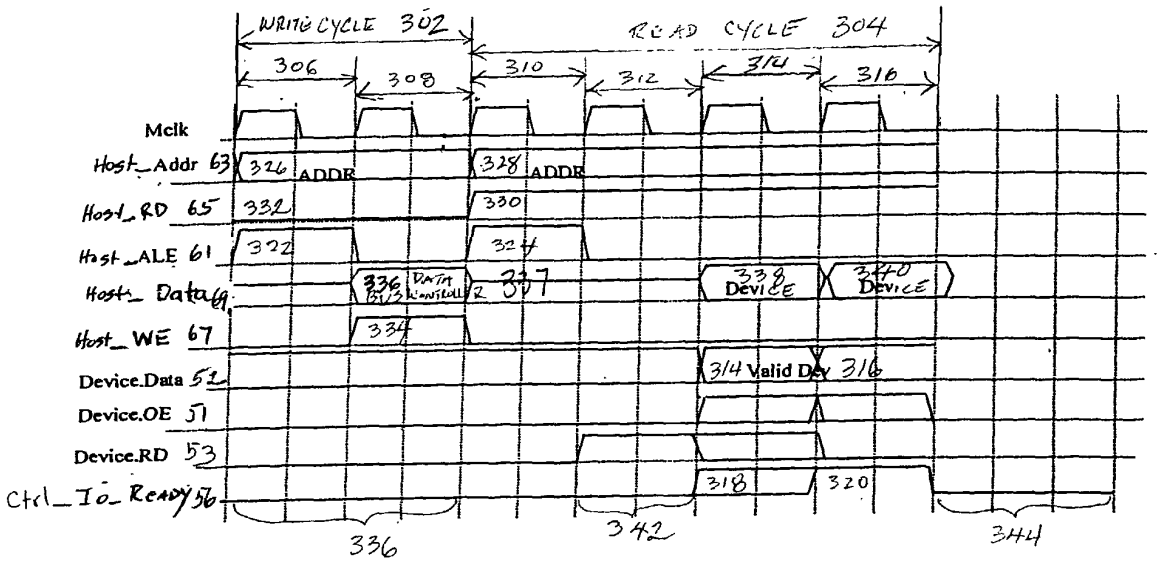
WRITE CYCLE 302
READ CYCLE 304
306
308
310
312
314
316
Mclk
Host_Addr 63
326
ADDR
328
ADDR
Host_RD 65
332
330
Host_ALE 61
322
324
Host_Data 69
336
DATA BUS
337
338
Device
340
Device
Host_WE 67
334
Device.Data 51
314 Valid Dev
316
Device.OE 51
Device.RD 53
Ctrl_Io_Ready 56
318
320
336
342
344

Fig. 13

Title: Multiple Channel Data Bus Control for Video Proces
Ap[redacted]ts: Xu Wang, Shuhua Xiang, Sha Li
Doc[redacted] No.: 22682-06323

HOST BIU 27a

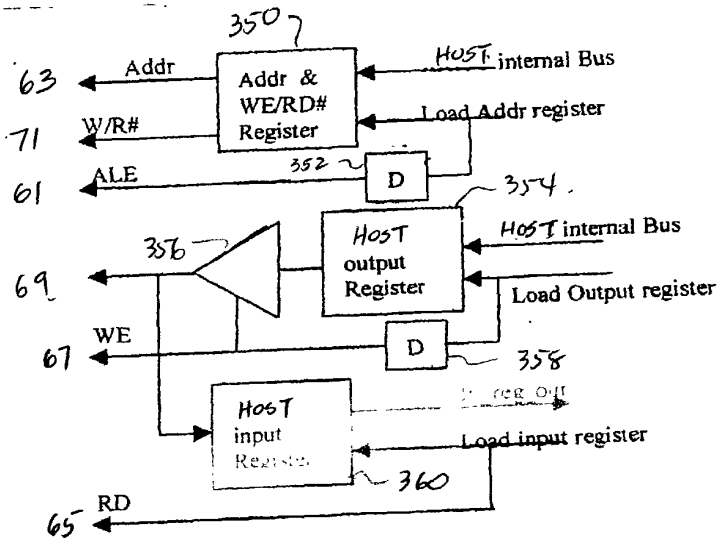

FIG. 14

DEVICE BIU 40a

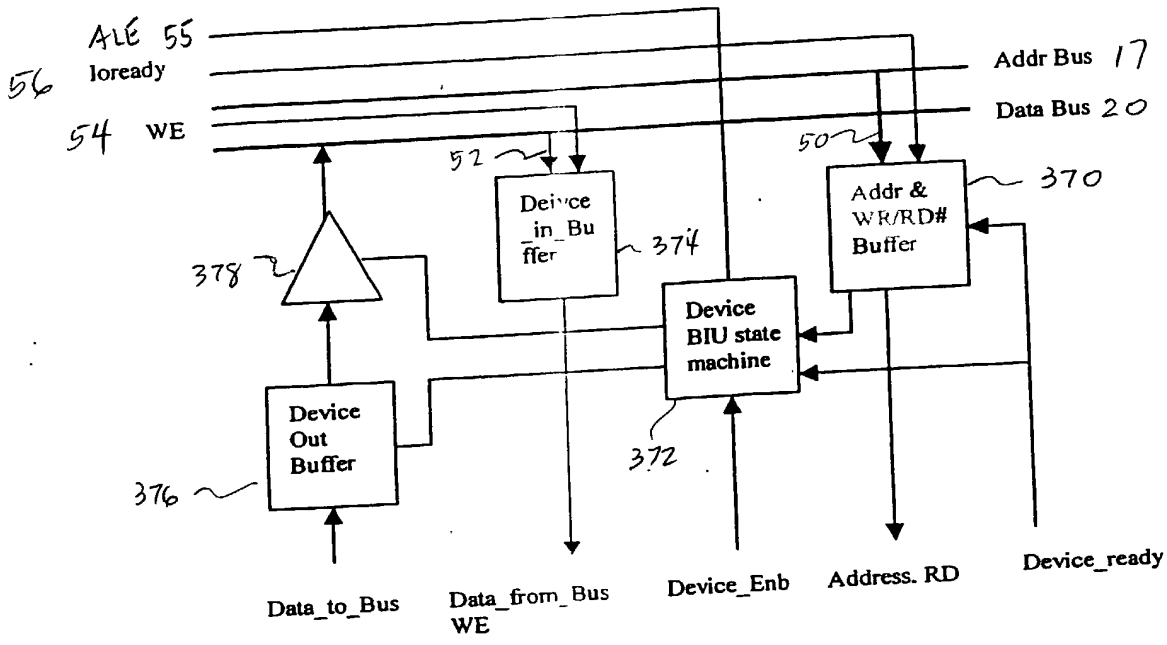

Fig. 15

SIGNAL FLOW DIAGRAM

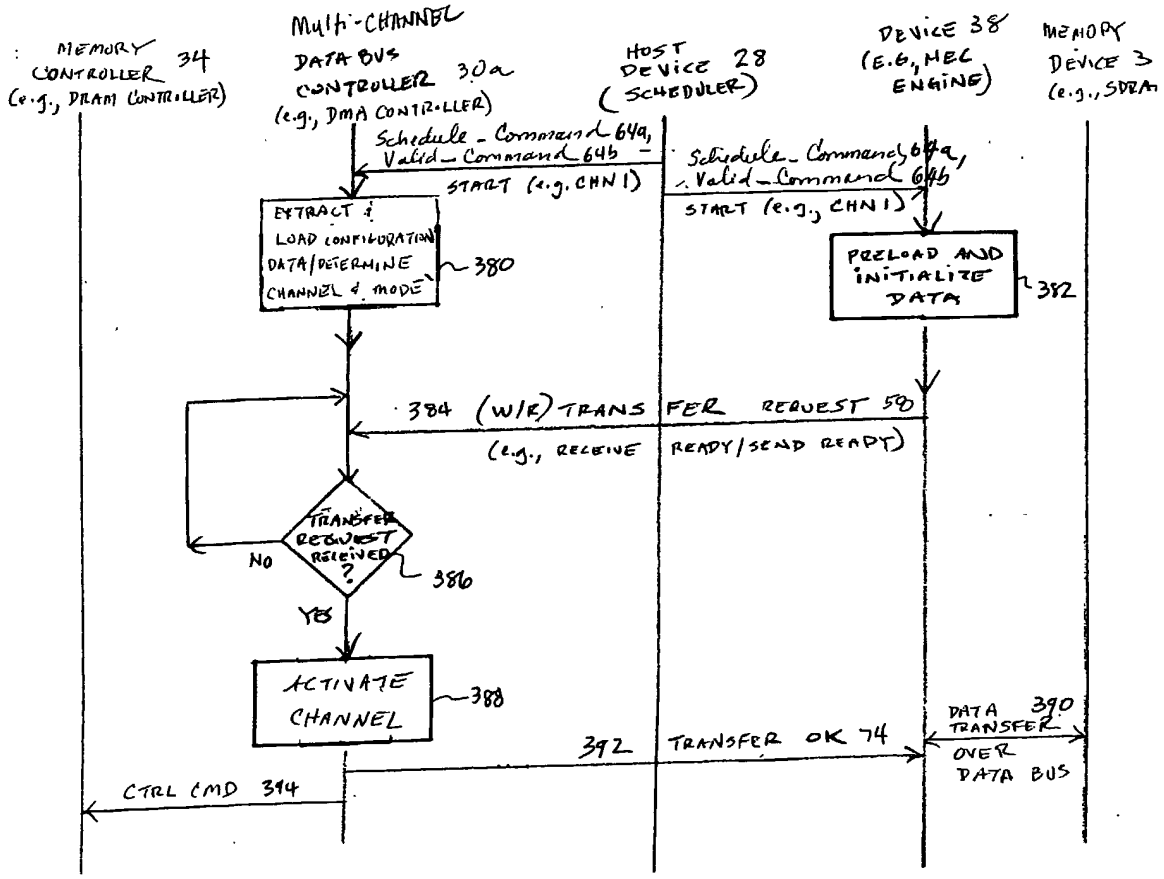

FIG. 16

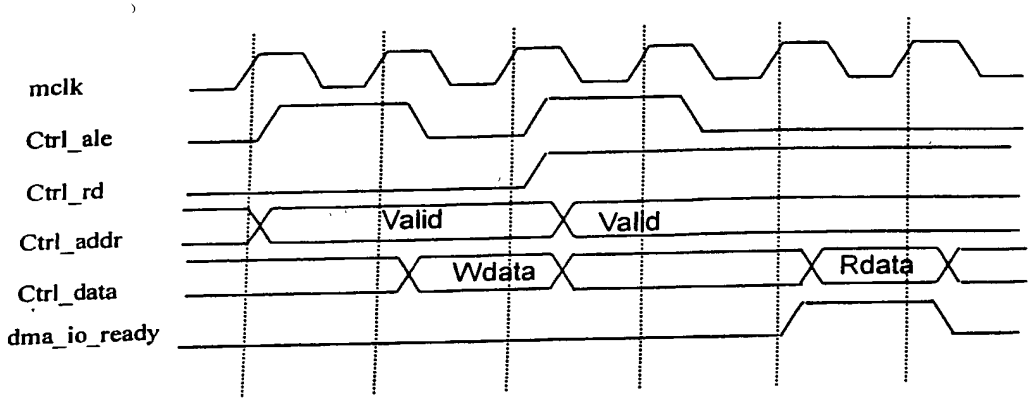
mclk
Ctrl_ale
Ctrl_rd
Ctrl_addr
Ctrl_data
dma_io_ready
Valid
Valid
Wdata
Rdata

Fig. 17

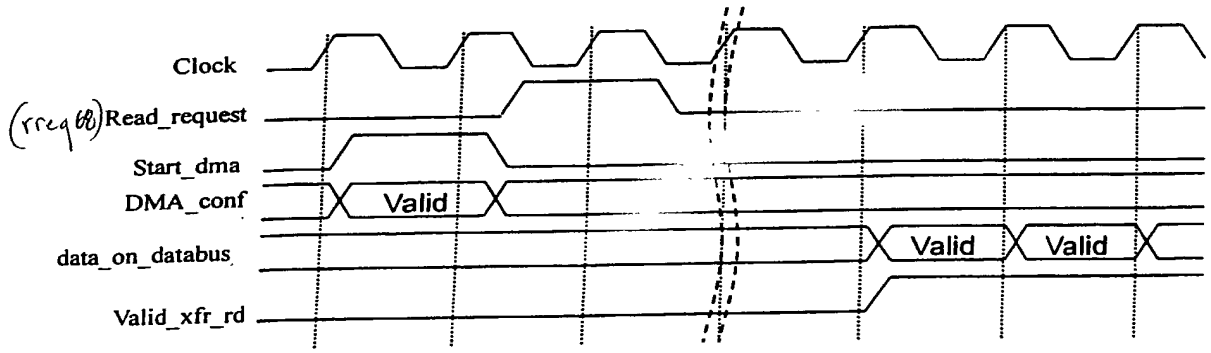
Clock
(rreq 68) Read_request
Start_dma
DMA_conf
data_on_databus
Valid_xfr_rd
Valid
Valid
Valid

Fig. 18

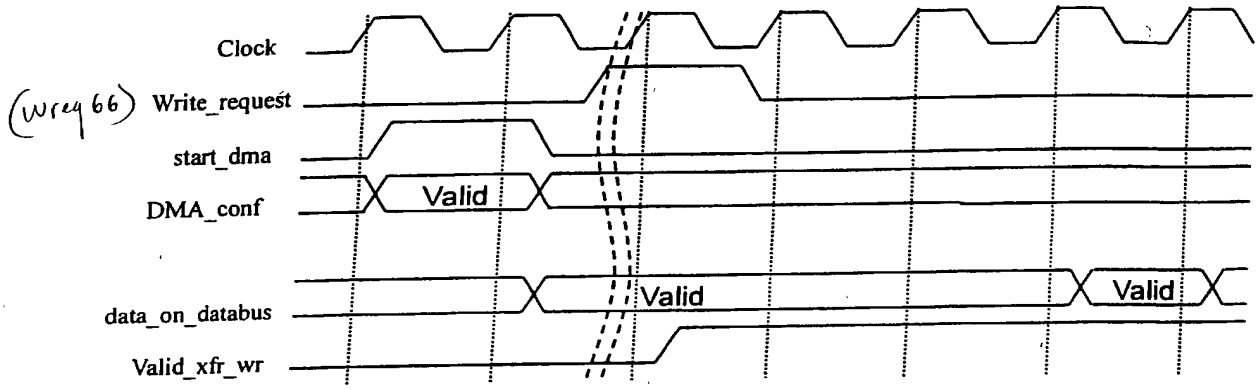
Clock
(wreq66) Write_request
start_dma
DMA_conf
Valid
data_on_databus
Valid
Valid
Valid_xfr_wr

Fig. 19

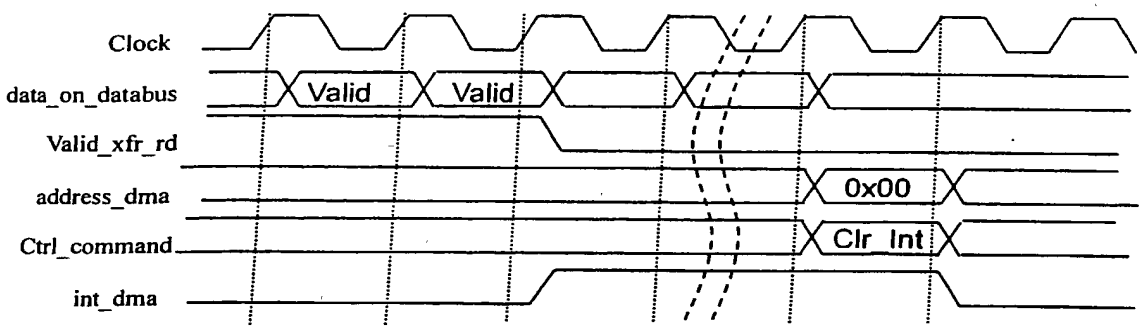
Clock
data_on_databus
Valid
Valid
Valid_xfr_rd
address_dma
0x00
Ctrl_command
Clr_Int
int_dma

Fig. 20

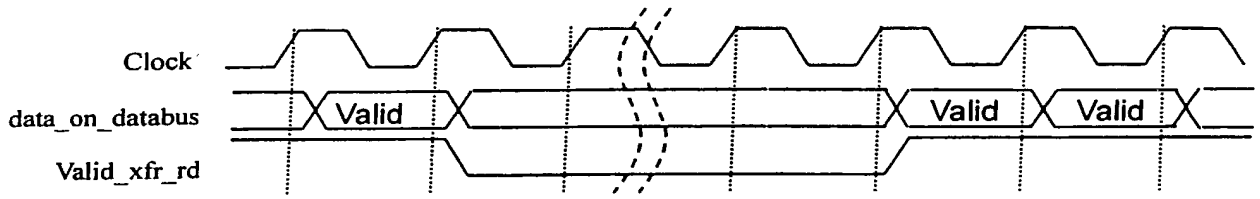
Clock
data_on_databus
Valid_xfr_rd
Valid
Valid
Valid

Fig. 21

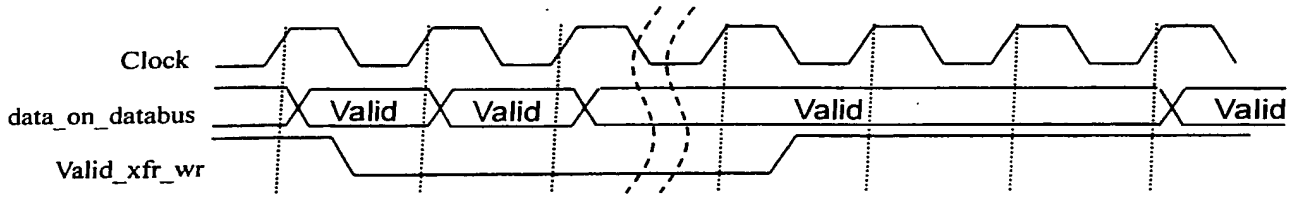
Clock
data_on_databus
Valid_xfr_wr
Valid
Valid
Valid
Valid

Fig. 22

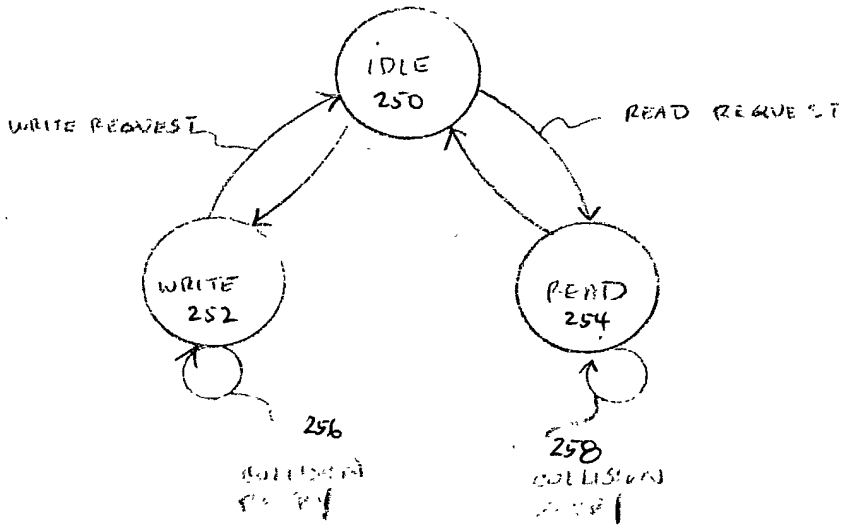
IDLE
250
WRITE REQUEST
READ REQUEST
WRITE
252
READ
254
256
258

FIG. 2B

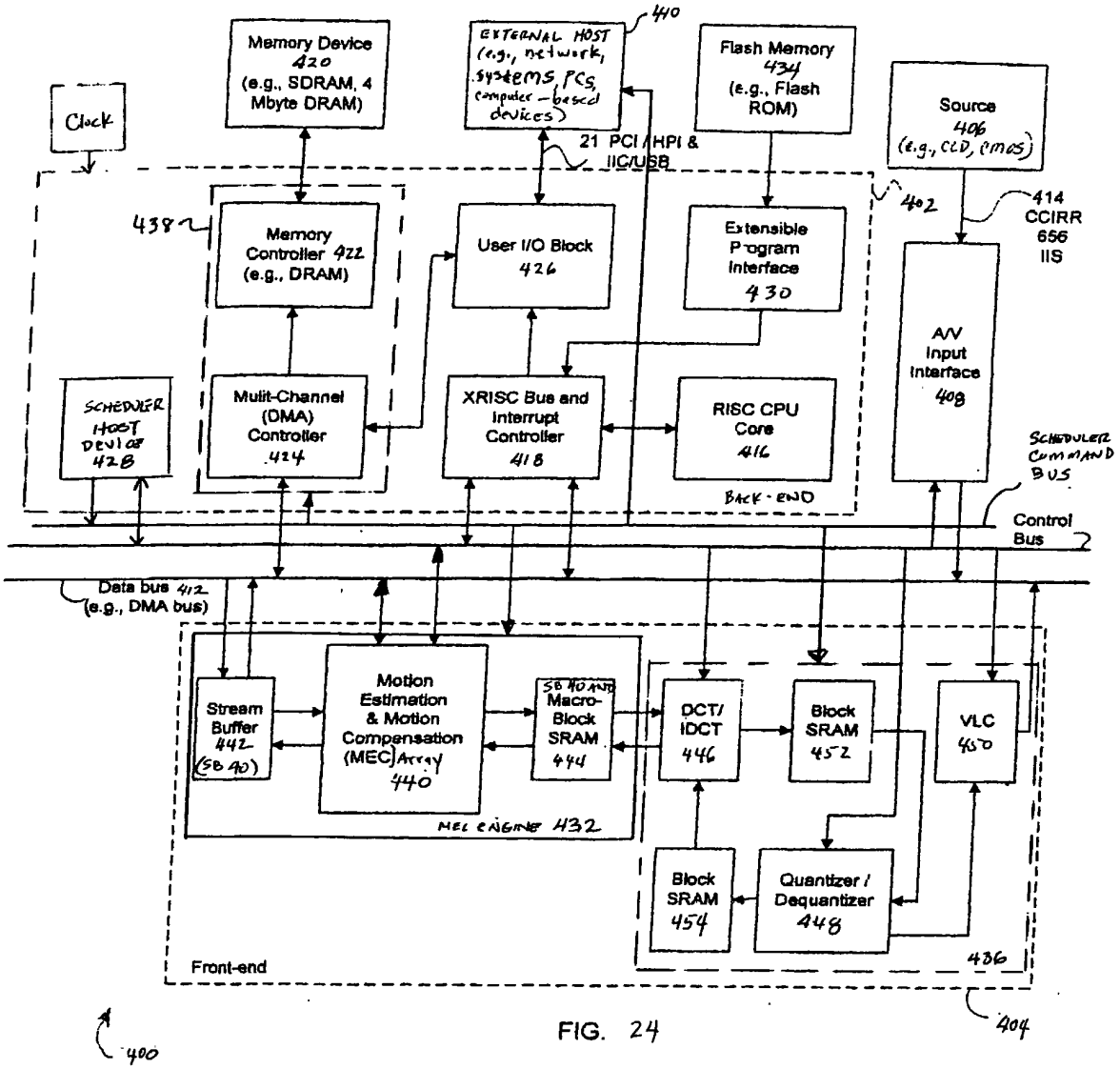
Memory Device
420
(e.g., SDRAM, 4 Mbyte DRAM)
EXTERNAL HOST (e.g., network, systems, PCs, computer-based devices)
410
Flash Memory
434
(e.g., Flash ROM)
Source
406
(e.g., CCD, CMOS)
Clock
21 PCI/HPI & IIC/USB
438
Memory Controller 422 (e.g., DRAM)
User I/O Block
426
Extensible Program Interface
430
402
414
CCIRR
656
IIS
A/V Input Interface
408
SCHEDULER HOST DEVICE 428
Mulit-Channel (DMA) Controller 424
XRISC Bus and Interrupt Controller
418
RISC CPU Core
416
BACK-END
SCHEDULER COMMAND BUS
Control Bus
Data bus 412
(e.g., DMA bus)
Stream Buffer
442
(SB 40)
Motion Estimation & Motion Compensation (MEC) Array
440
SB 40 and Macro-Block SRAM
444
MEC ENGINE 432
DCT/IDCT
446
Block SRAM
452
VLC
450
Block SRAM
454
Quantizer / Dequantizer
448
436
Front-end
404
400

FIG. 24

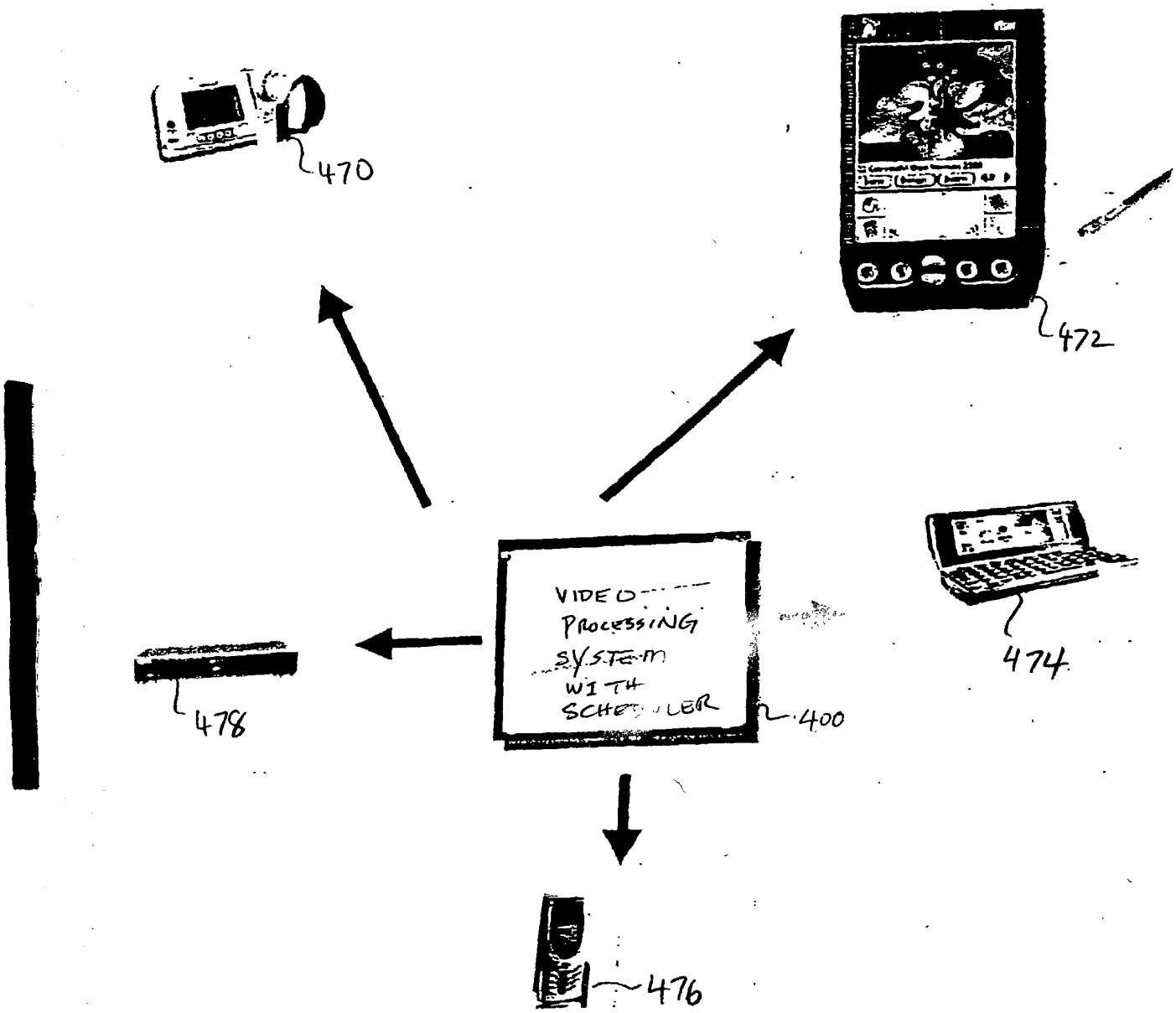
470
472
474
476
478
VIDEO PROCESSING SYSTEM WITH SCHEDULER
400

FIG. 25

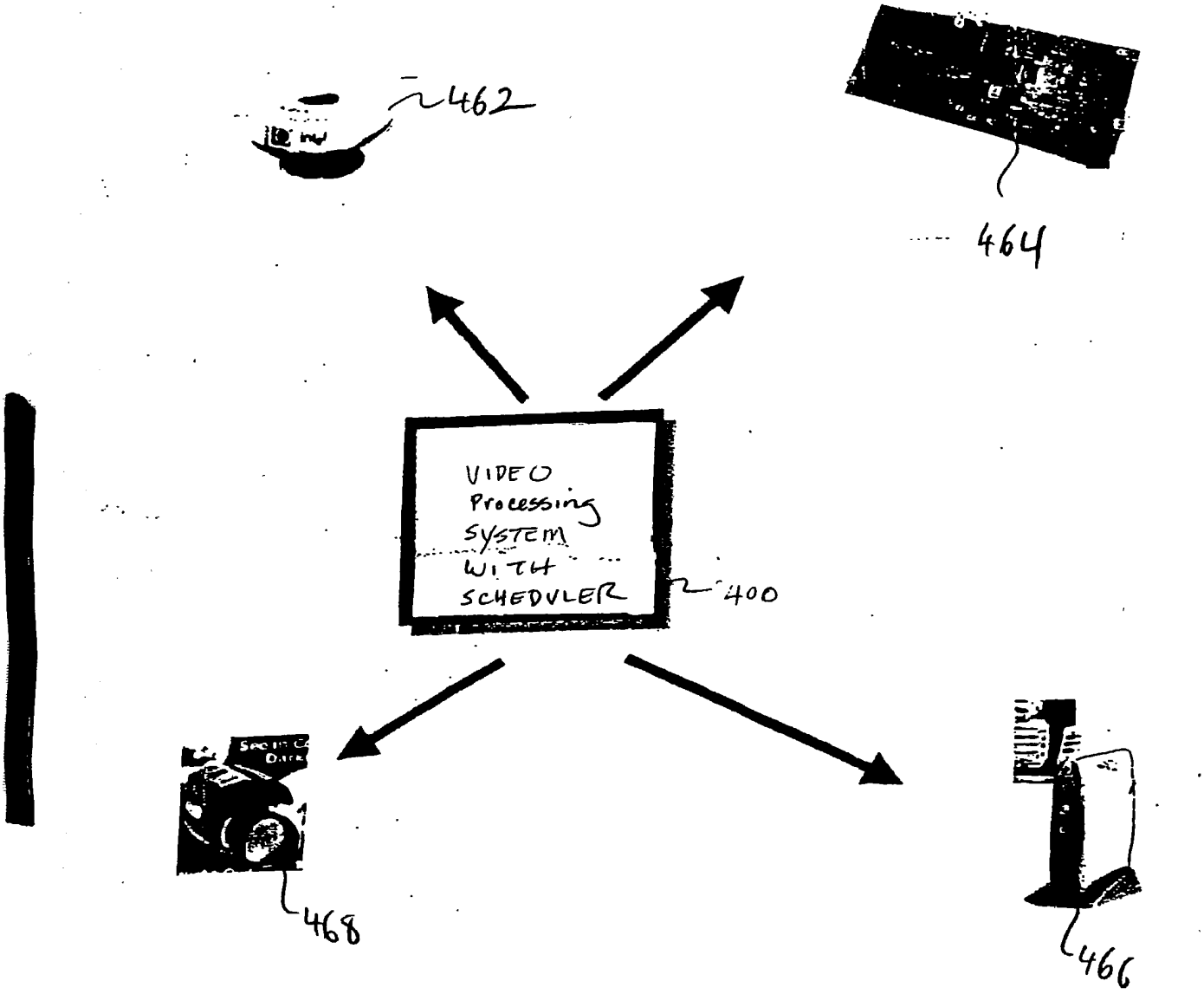

FIG. 26